



# 64K x 32 Synchronous-Pipelined Cache RAM

## Features

- Supports 133-MHz bus for Pentium® and PowerPC™ operations with zero wait states
- Fully registered inputs and outputs for pipelined operation
- 64K x 32 common I/O architecture
- Single 3.3V power supply
- Fast clock-to-output times
  - 4.2 ns (for 133-MHz device)
  - 5.5 ns (for 100-MHz device)
- User-selectable burst counter supporting Intel® Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- JEDEC-standard 100-lead TQFP pinout
- “ZZ” Sleep Mode option and Stop Clock option

## Functional Description

The CY7C1329 is a 3.3V, 64K by 32 synchronous-pipelined cache SRAM designed to support zero wait state secondary cache with minimal glue logic.

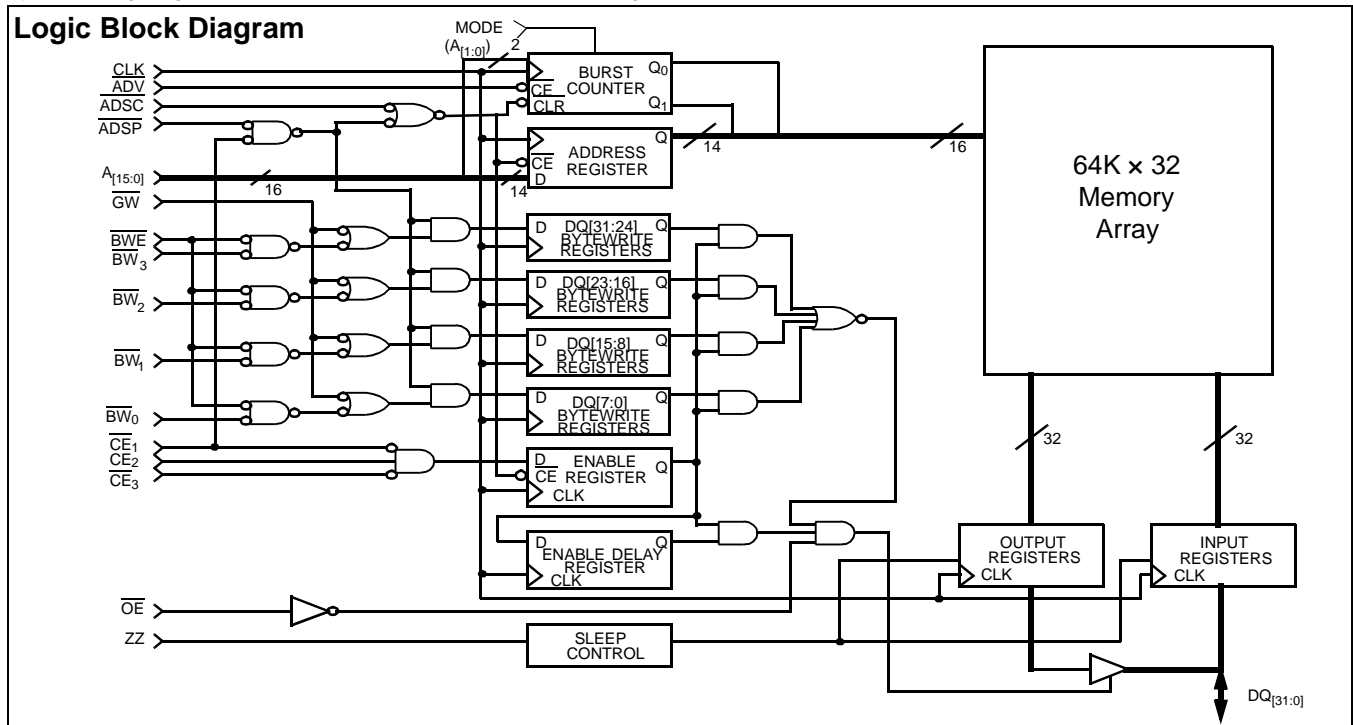
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through

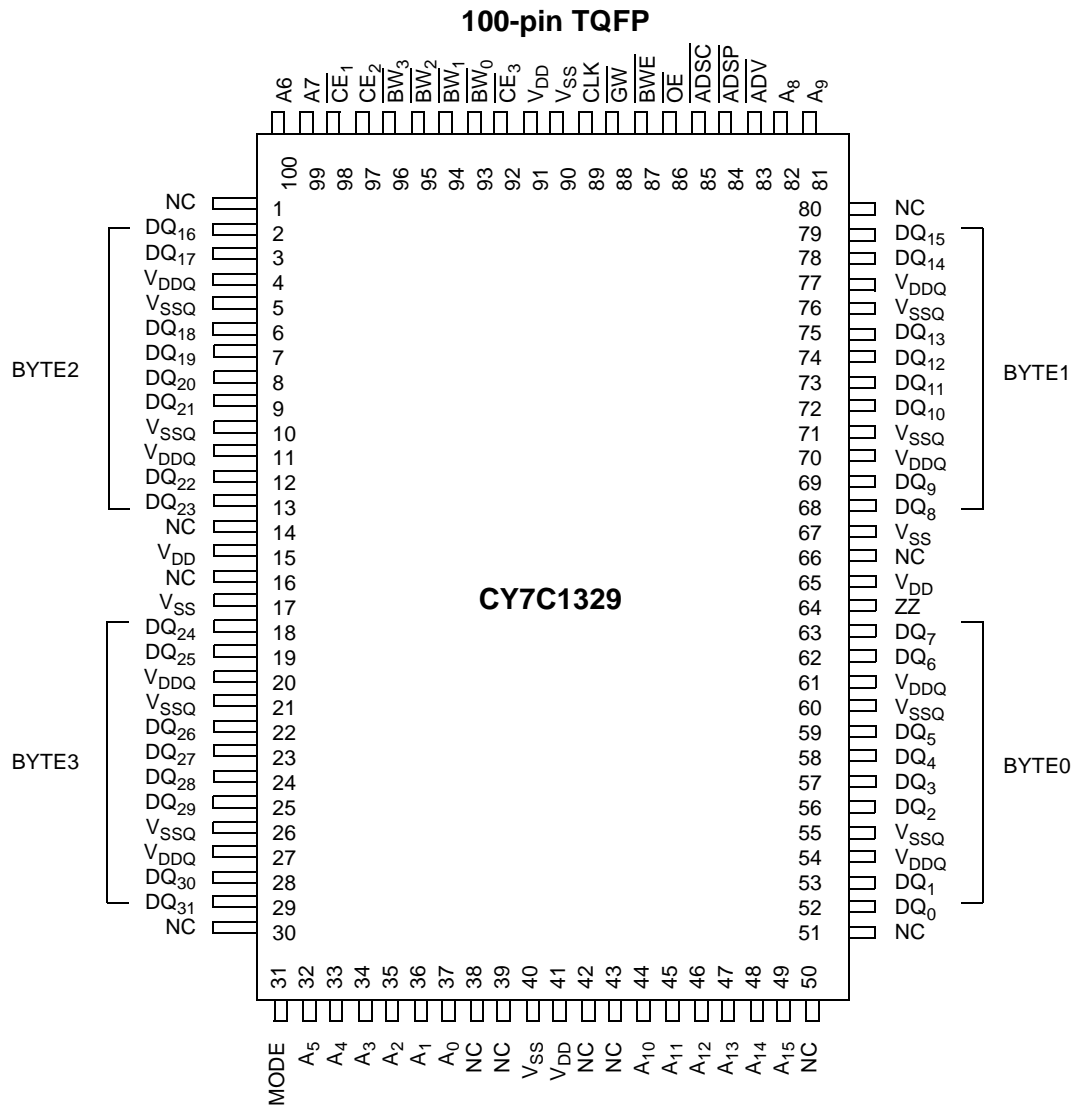
output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 4.2 ns (133-MHz device).

The CY7C1329 supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC) at clock rise. Address advancement through the burst sequence is controlled by the ADV input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the four Byte Write Select (BW<sub>[3:0]</sub>) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion,  $\overline{OE}$  is masked during the first clock of a Read cycle when emerging from a deselected state.



**Pin Configuration**

**Selection Guide**

		<b>7C1329-133</b>	<b>7C1329-100</b>	<b>Unit</b>
Maximum Access Time		4.2	5.5	ns
Maximum Operating Current	Commercial	325	310	mA
Maximum CMOS Standby Current	Commercial	5	5	mA

**Pin Definitions**

Pin Number	Name	I/O	Description
49–44, 81, 82, 99, 100, 32–37	A <sub>[15:0]</sub>	Input-Synchronous	<b>Address Inputs used to select one of the 64K address locations.</b> Sampled at the rising edge of the CLK if $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is active LOW, and $\overline{\text{CE}}_1$ , $\text{CE}_2$ , and $\overline{\text{CE}}_3$ are sampled active. A <sub>[1:0]</sub> feed the 2-bit counter.
96–93	BW <sub>[3:0]</sub>	Input-Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with $\overline{\text{BWE}}$ to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK.
88	GW	Input-Synchronous	<b>Global Write Enable Input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global Write is conducted (ALL bytes are written, regardless of the values on $\overline{\text{BW}}_{[3:0]}$ and $\overline{\text{BWE}}$ ).
87	BWE	Input-Synchronous	<b>Byte Write Enable Input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write.
89	CLK	Input-Clock	<b>Clock input. Used to capture all synchronous inputs to the device.</b> Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
98	CE <sub>1</sub>	Input-Synchronous	<b>Chip Enable 1 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_2$ and $\overline{\text{CE}}_3$ to select/deselect the device. ADSP is ignored if $\overline{\text{CE}}_1$ is HIGH.
97	CE <sub>2</sub>	Input-Synchronous	<b>Chip Enable 2 Input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device.
92	CE <sub>3</sub>	Input-Synchronous	<b>Chip Enable 3 Input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ to select/deselect the device.
86	OE	Input-Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{\text{OE}}$ is masked during the first clock of a Read cycle when emerging from a deselected state.
83	ADV	Input-Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
84	ADSP	Input-Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK.</b> When asserted LOW, A <sub>[15:0]</sub> is captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized. $\overline{\text{ADSP}}$ is ignored when $\overline{\text{CE}}_1$ is deasserted HIGH.
85	ADSC	Input-Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK.</b> When asserted LOW, A <sub>[15:0]</sub> is captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized.
64	ZZ	Input-Asynchronous	<b>ZZ “sleep” Input.</b> This active HIGH input places the device in a non-time-critical “sleep” condition with data integrity preserved.
29, 28, 25–22, 19, 18, 13, 12, 9–6, 3, 2, 79, 78, 75–72, 69, 68, 63, 62 59–56, 53, 52	DQ <sub>[31:0]</sub>	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A <sub>[15:0]</sub> during the <u>previous</u> clock rise of the Read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>[31:0]</sub> are placed in a three-state condition.
15, 41, 65, 91	V <sub>DD</sub>	Power Supply	<b>Power supply inputs to the core of the device.</b> Should be connected to 3.3V power supply.
17, 40, 67, 90	V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b> Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	V <sub>DDQ</sub>	I/O Power Supply	<b>Power supply for the I/O circuitry.</b> Should be connected to a 3.3V power supply.
5, 10, 21, 26, 55, 60, 71, 76	V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O circuitry.</b> Should be connected to ground of the system.
31	MODE	Input-Static	<b>Selects burst order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DDQ</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
1, 14, 16, 30, 38, 39, 42, 43, 50, 51, 66, 80	NC	–	No Connects.

## Introduction

### Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CO}$ ) is 4.2 ns (133-MHz device).

The CY7C1329 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ( $BW_{[3:0]}$ ) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) provide for easy bank selection and output three-state control. ADSP is ignored if  $CE_1$  is HIGH.

#### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2)  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$  are all asserted active, and (3) the Write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if  $CE_1$  is HIGH. The address presented to the address inputs ( $A_{[15:0]}$ ) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 4.2 ns (133-MHz device) if  $\overline{OE}$  is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the  $\overline{OE}$  signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will three-state immediately.

#### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2)  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$  are all asserted active. The address presented to  $A_{[15:0]}$  is loaded into the address register and the address advancement logic while being delivered to the RAM core. The Write signals (GW, BWE, and  $BW_0$ – $BW_3$ ) and ADV inputs are ignored during this first cycle.

ADSP triggered Write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the  $DQ_{[31:0]}$  inputs is written into the corre-

sponding address location in the RAM core. If  $\overline{GW}$  is HIGH, then the Write operation is controlled by BWE and  $BW_{[3:0]}$  signals. The CY7C1329 provides Byte Write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write ( $BW_{[3:0]}$ ) input will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1329 is a common I/O device, the Output Enable ( $\overline{OE}$ ) must be deasserted HIGH before presenting data to the  $DQ_{[31:0]}$  inputs. Doing so will three-state the output drivers. As a safety precaution,  $DQ_{[31:0]}$  are automatically three-stated whenever a Write cycle is detected, regardless of the state of  $\overline{OE}$ .

#### Single Write Accesses Initiated by $\overline{ADSC}$

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3)  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$  are all asserted active, and (4) the appropriate combination of the Write inputs ( $\overline{GW}$ , BWE, and  $BW_{[3:0]}$ ) are asserted active to conduct a Write to the desired byte(s). ADSC triggered Write accesses require a single clock cycle to complete. The address presented to  $A_{[15:0]}$  is loaded into the address register and the address advancement logic while being delivered to the RAM core. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to the  $DQ_{[31:0]}$  is written into the corresponding address location in the RAM core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A Synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1329 is a common I/O device, the Output Enable ( $\overline{OE}$ ) must be deasserted HIGH before presenting data to the  $DQ_{[31:0]}$  inputs. Doing so will three-state the output drivers. As a safety precaution,  $DQ_{[31:0]}$  are automatically three-stated whenever a Write cycle is detected, regardless of the state of  $\overline{OE}$ .

## Burst Sequences

The CY7C1329 provides a two-bit wraparound counter, fed by  $A_{[1:0]}$ , that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting  $\overline{ADV}$  LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

### Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Linear Burst Sequence**

First Address	Second Address	Third Address	Fourth Address
A <sub>[1:0]</sub>	A <sub>[1:0]</sub>	A <sub>[1:0]</sub>	A <sub>[1:0]</sub>
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**Sleep Mode**

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode.  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ , ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min.	Max.	Unit
$I_{DDZZ}$	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		3	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

**Cycle Descriptions<sup>[1,2,3]</sup>**

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	$\overline{CE}_2$	$\overline{CE}_1$	ADSP	ADSC	ADV	OE	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
ZZ "sleep"	None	H	X	X	X	X	X	X	X	Hi-Z	X

**Notes:**

1. X = "Don't Care," 1 = HIGH, 0 = LOW.
2. Write is defined by  $\overline{BWE}$ ,  $BW_{[3:0]}$ , and  $\overline{GW}$ . See Write Cycle Descriptions table.
3. The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.

**Write Cycle Descriptions<sup>[4,5,6]</sup>**

Function	GW	BWE	BW <sub>3</sub>	BW <sub>2</sub>	BW <sub>1</sub>	BW <sub>0</sub>
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 – DQ <sub>[7:0]</sub>	1	0	1	1	1	0
Write Byte 1 – DQ <sub>[15:8]</sub>	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 – DQ <sub>[23:16]</sub>	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - DQ <sub>[31:24]</sub>	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied..... -55°C to +125°C  
 Supply Voltage on V<sub>DD</sub> Relative to GND..... -0.5V to +4.6V  
 DC Voltage Applied to Outputs  
 in High-Z State<sup>[7]</sup> ..... -0.5V to V<sub>DDQ</sub> + 0.5V

DC Input Voltage<sup>[7]</sup>..... -0.5V to V<sub>DDQ</sub> + 0.5V  
 Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[8]</sup>	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V -5%/+10%	3.3V -5%/+10%

**Notes:**

- X = "Don't Care," 1 = Logic HIGH, 0 = Logic LOW.
- The SRAM always initiates a Read cycle when ADSP asserted, regardless of the state of  $\overline{\text{GW}}$ ,  $\overline{\text{BWE}}$ , or  $\overline{\text{BW}}_{[3:0]}$ . Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result,  $\overline{\text{OE}}$  must be driven HIGH prior to the start of the Write cycle to allow the outputs to three-state.  $\overline{\text{OE}}$  is a "don't care" for the remainder of the Write cycle.
- $\overline{\text{OE}}$  is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle DQ = High-Z when  $\overline{\text{OE}}$  is inactive or when the device is deselected, and DQ = data when  $\overline{\text{OE}}$  is active.
- Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the case temperature.

**Electrical Characteristics** Over the Operating Range

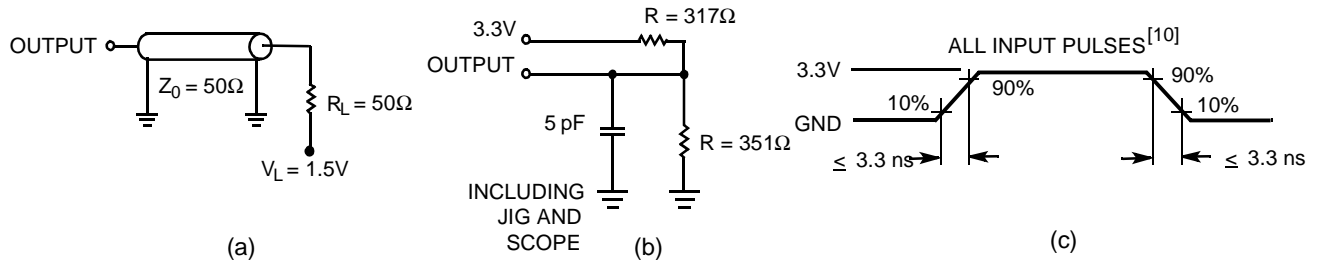
Parameter	Description	Test Conditions		Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage	3.3V -5%/+10%		3.135	3.6	V
V <sub>DDQ</sub>	I/O Supply Voltage	3.3V -5%/+10%		3.135	3.6	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.0	V <sub>DDQ</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[7]</sup>			-0.3	0.8	V
I <sub>X</sub>	Input Load Current Except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>		-5	5	μA
		Input Current of MODE	Input = V <sub>SS</sub>	-30		μA
	Input = V <sub>DDQ</sub>			5	μA	
	Input Current of ZZ	Input = V <sub>SS</sub>	-5		μA	
Input = V <sub>DDQ</sub>			30	μA		
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled		-5	5	μA
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz		325	mA
			10-ns cycle, 100 MHz		260	mA
I <sub>SB1</sub>	Automatic CS Power-down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz		60	mA
			10-ns cycle, 100 MHz		50	mA
I <sub>SB2</sub>	Automatic CS Power-down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = 0	All speeds		5	mA
I <sub>SB3</sub>	Automatic CS Power-down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, or V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5-ns cycle, 133 MHz		40	mA
			10-ns cycle, 100 MHz		30	mA
I <sub>SB4</sub>	Automatic CS Power-down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0			25	mA

**Capacitance<sup>[9]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = 3.3V, V <sub>DDQ</sub> = 3.3V	4	pF
C <sub>CLK</sub>	Clock Input Capacitance		4	pF
C <sub>I/O</sub>	Input/Output Capacitance		4	pF

**Note:**

9. Tested initially and after any design or process changes that may affect these parameters.

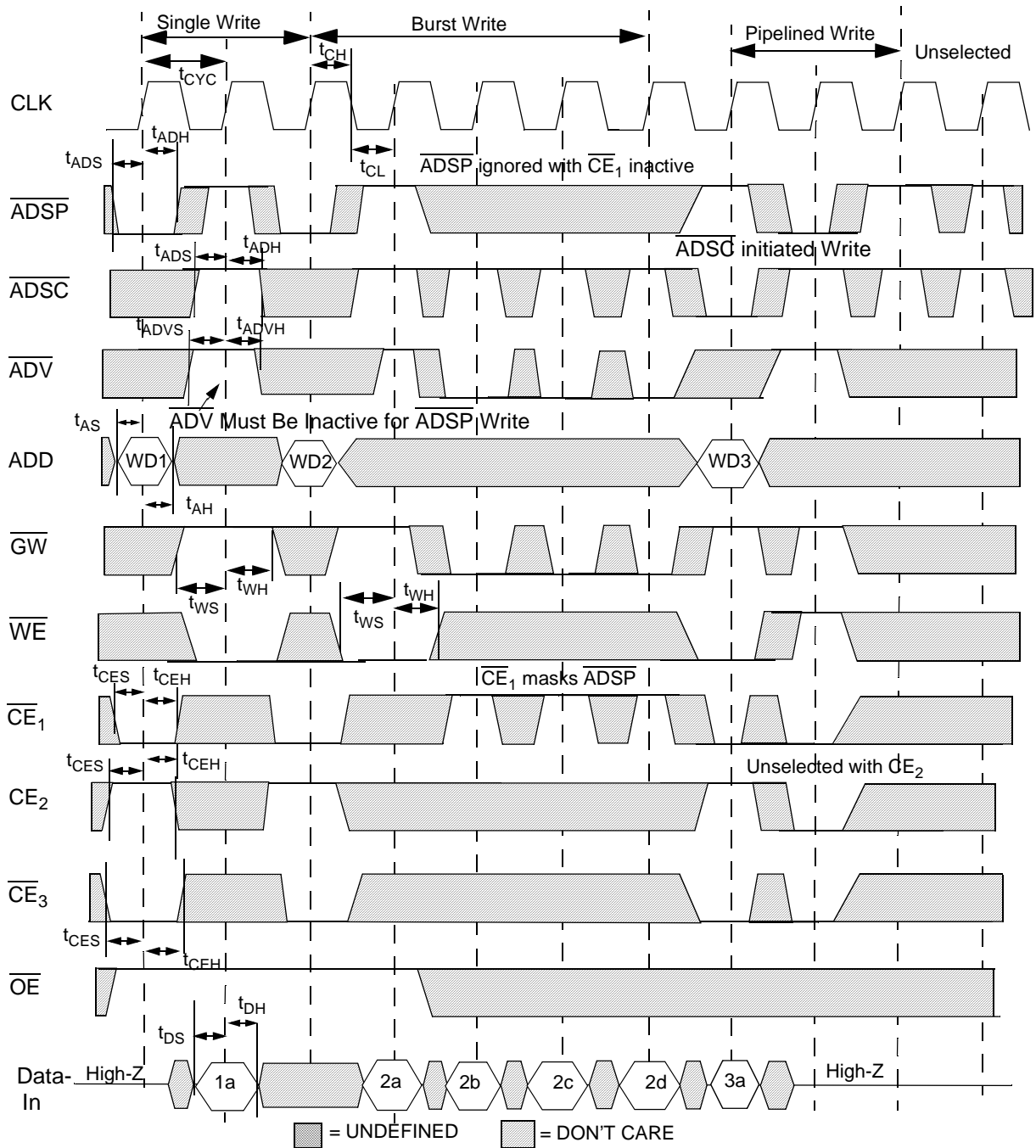
**AC Test Loads and Waveforms**

**Switching Characteristics** Over the Operating Range<sup>[11,12,13]</sup>

Parameter	Description	-133		-100		-75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CYC}$	Clock Cycle Time	7.5		10		13.3		ns
$t_{CH}$	Clock HIGH	1.9		3.2		5.0		ns
$t_{CL}$	Clock LOW	1.9		3.2		5.0		ns
$t_{AS}$	Address Set-up Before CLK Rise	1.5		2.5		2.5		ns
$t_{AH}$	Address Hold After CLK Rise	0.5		0.5		0.5		ns
$t_{CO}$	Data Output Valid After CLK Rise		4.2		5.0		7.0	ns
$t_{DOH}$	Data Output Hold After CLK Rise	1.5		2.0		2.5		ns
$t_{ADS}$	ADSP, ADSC Set-up Before CLK Rise	1.5		2.5		2.5		ns
$t_{ADH}$	ADSP, ADSC Hold After CLK Rise	0.5		0.5		0.5		ns
$t_{WES}$	BWE, GW, BW[3:0] Set-up Before CLK Rise	1.5		2.5		2.5		ns
$t_{WEH}$	BWE, GW, BW[3:0] Hold After CLK Rise	0.5		0.5		0.5		ns
$t_{ADVS}$	ADV Set-up Before CLK Rise	1.5		2.5		2.5		ns
$t_{ADVH}$	ADV Hold After CLK Rise	0.5		0.5		0.5		ns
$t_{DS}$	Data Input Set-up Before CLK Rise	1.5		2.5		2.5		ns
$t_{DH}$	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
$t_{CES}$	Chip Select Set-up	1.5		2.5		2.5		ns
$t_{CEH}$	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
$t_{CHZ}$	Clock to High-Z <sup>[12]</sup>	1.5	3.5	1.5	5	2	6	ns
$t_{CLZ}$	Clock to Low-Z <sup>[12]</sup>	0		0		0		ns
$t_{EOHZ}$	OE HIGH to Output High-Z <sup>[12, 13]</sup>		3.5		5.5		6	ns
$t_{EOLZ}$	OE LOW to Output Low-Z <sup>[12, 13]</sup>	0		0		0		ns
$t_{EOV}$	OE LOW to Output Valid <sup>[12]</sup>		4.2		5.0		6	ns

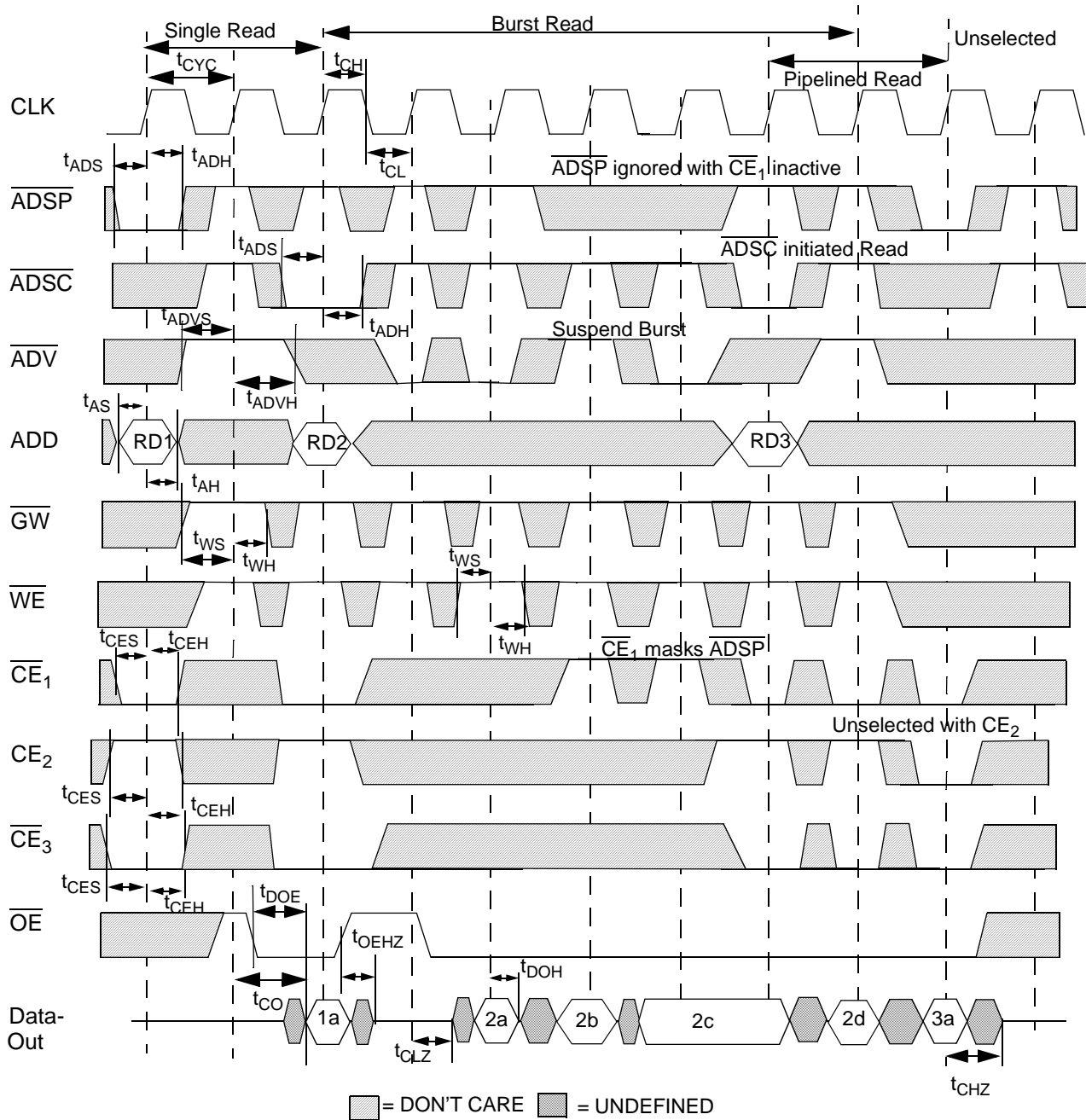
**Notes:**

- Input waveform should have a slew rate of 1V/ns.
- Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance. Shown in (a) and (b) of AC Test Loads.
- $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{EOV}$ ,  $t_{EOLZ}$ , and  $t_{EOHZ}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- At any given voltage and temperature,  $t_{EOHZ}$  is less than  $t_{EOLZ}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$ .

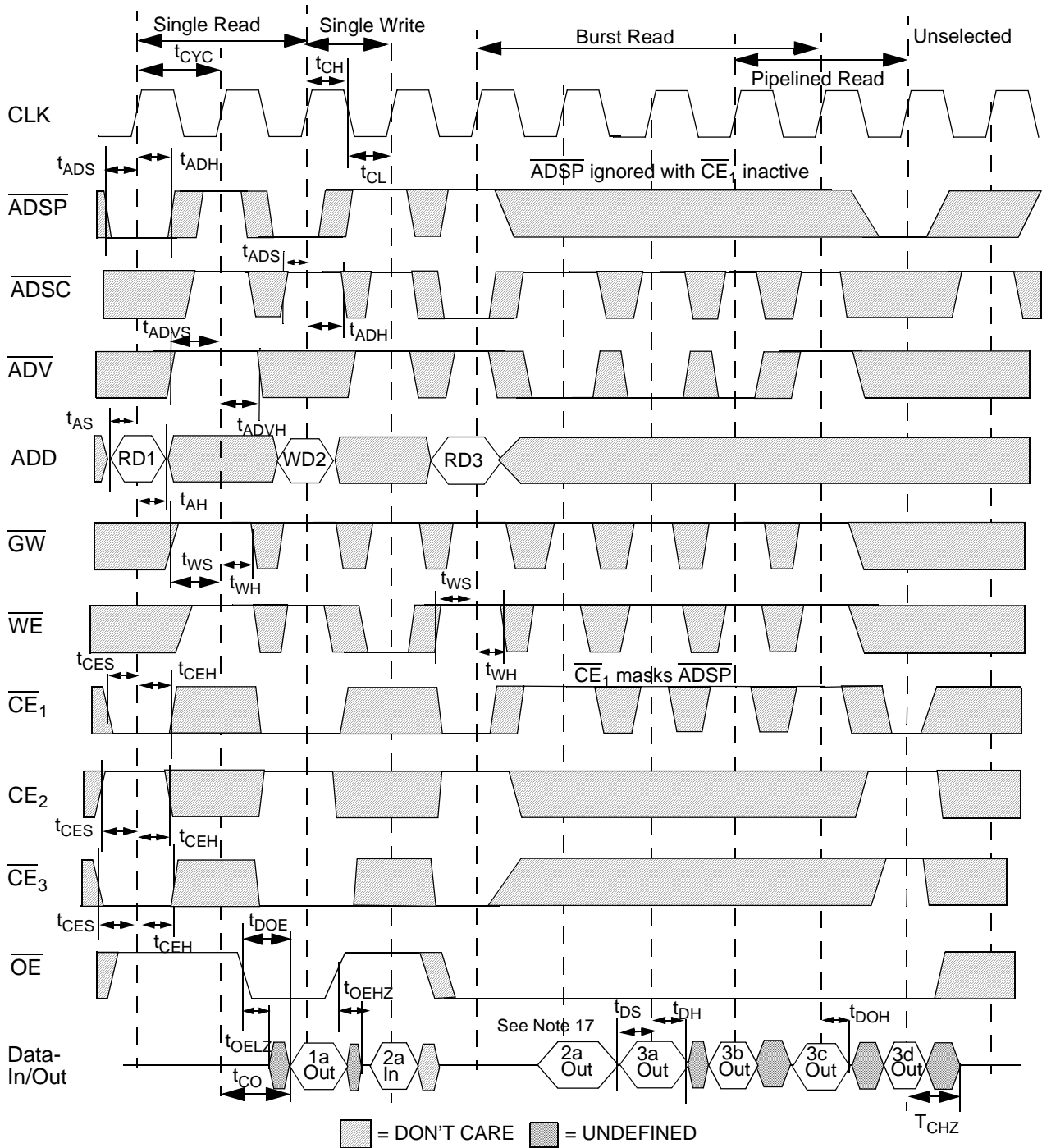


**Switching Waveforms**
**Write Cycle Timing<sup>[14, 15]</sup>**

**Notes:**

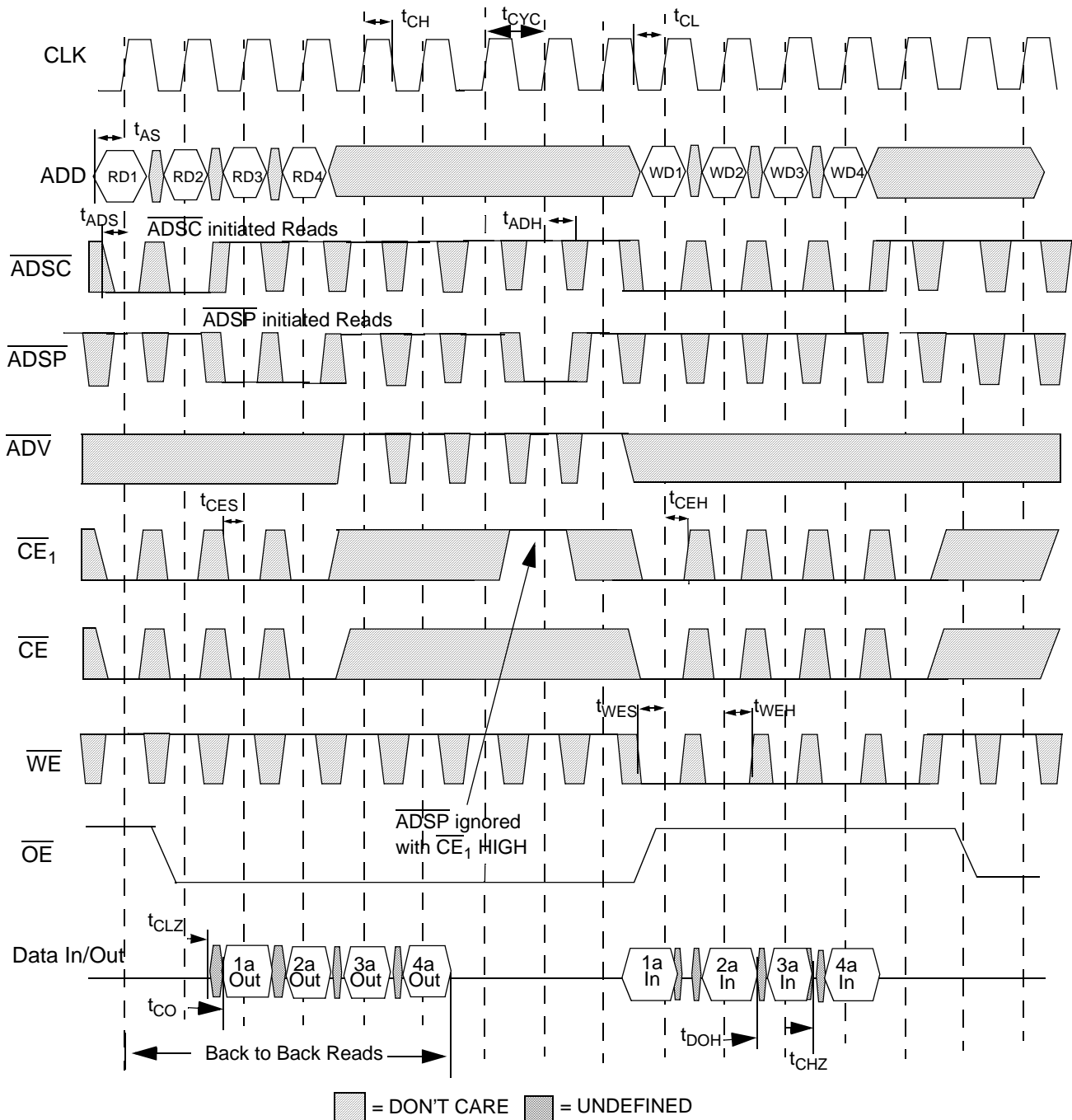
- 14.  $\overline{WE}$  is the combination of  $\overline{BWE}$ ,  $\overline{BW}_{[3:0]}$  and  $\overline{GW}$  to define a Write cycle (see Write Cycle Descriptions table).
- 15.  $WD_x$  stands for Write Data to Address X.

**Switching Waveforms (continued)**  
**Read Cycle Timing<sup>[14, 16]</sup>**

**Note:**

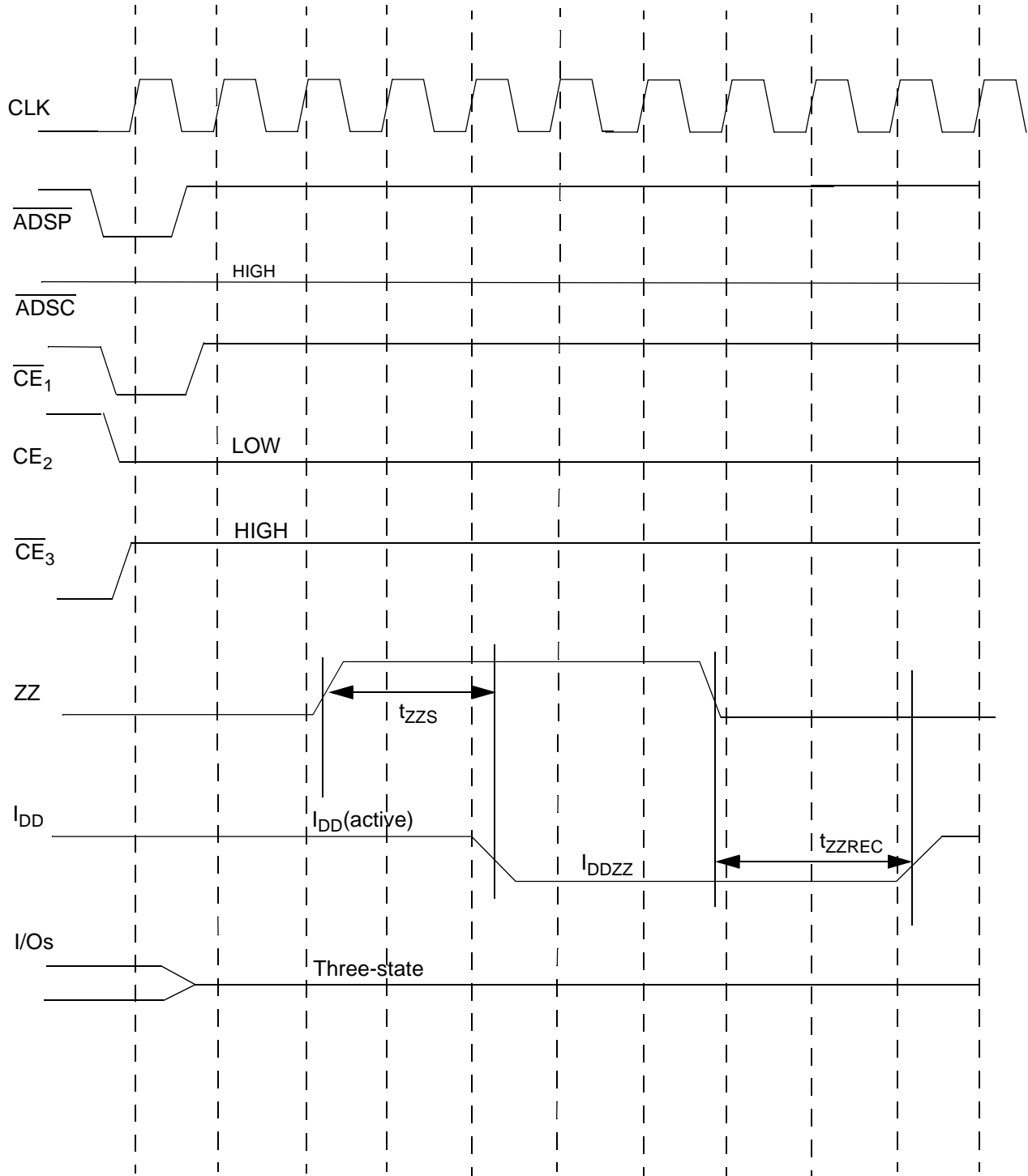
16. RDx stands for Read Data from Address X.

**Switching Waveforms** (continued)  
**Read/Write Cycle Timing**<sup>[14,15,16, 17]</sup>


**Note:**  
 17. Data bus is driven by SRAM, but data is not guaranteed.

**Switching Waveforms (continued)**  
**Pipeline Timing<sup>[18,19]</sup>**

**Notes:**

18. Device originally deselected.
19. CE is the combination of  $\overline{CE}_2$  and  $\overline{CE}_3$ . All chip selects need to be active in order to select the device.

**Switching Waveforms** (continued)  
**ZZ Mode Timing**<sup>[20, 21]</sup>

**Notes:**

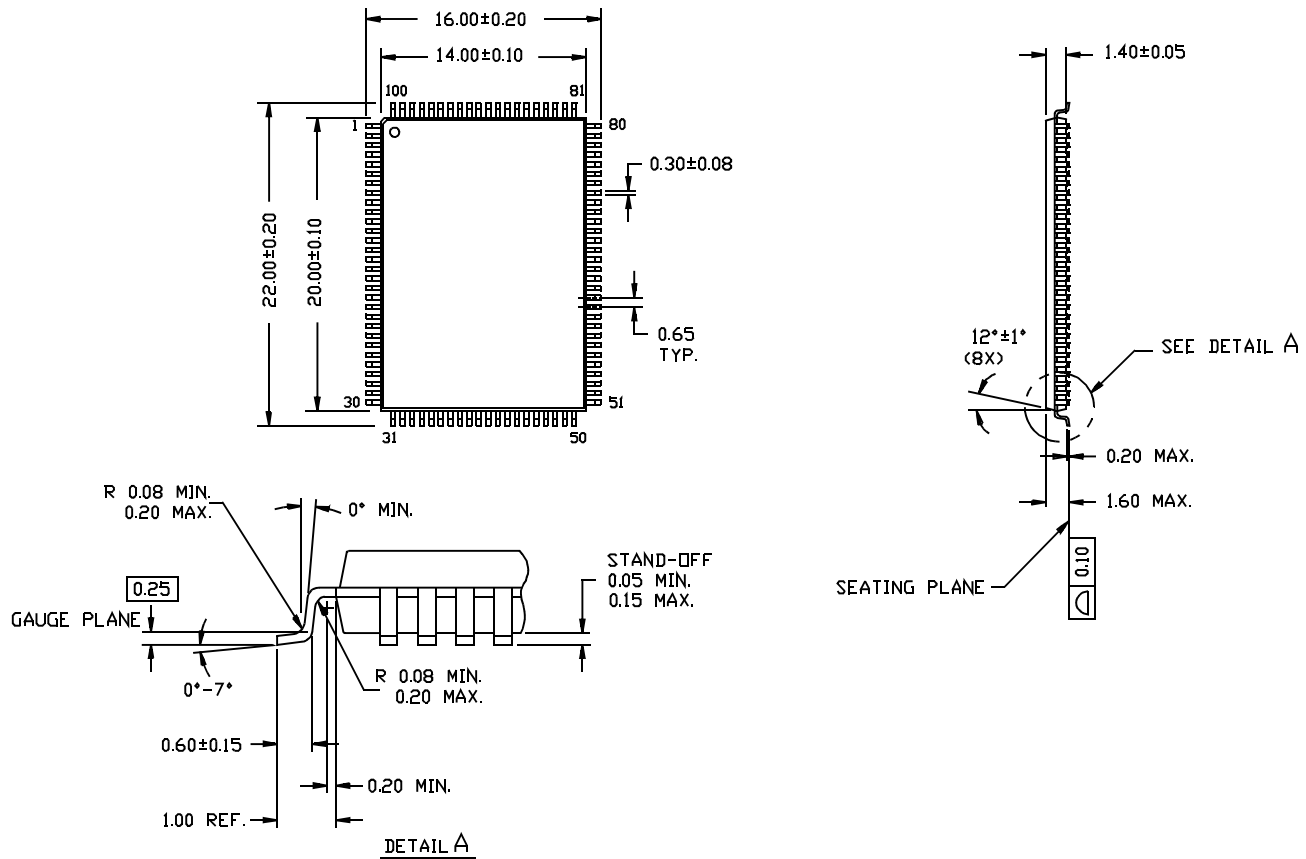
- 20. Device must be deselected when entering ZZ mode. See Cycle Description table for all possible signal conditions to deselect the device.
- 21. I/Os are in three-state when exiting ZZ sleep mode.

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1329-133AC	A101	100-lead Thin Quad Flat Pack	Commercial
100	CY7C1329-100AC	A101	100-lead Thin Quad Flat Pack	

**Package Diagram**
**100-lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101**

DIMENSIONS ARE IN MILLIMETERS.



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REV.	ECN NO	Issue Date	Orig. of Change	Description of changes
**	114388	03/25/02	DSG	Change from Spec number: 38-00561 to 38-05279
*A	114499	04/11/02	GLC	Changed to 1.5 set-up